

**APPLICATION
FOR
UNITED STATES LETTERS PATENT**

**TITLE: EVALUATING THE QUALITY
 OF A CONTACT PLUG FILL**

**INVENTORS: Swaminathan Sivakumar, Oleg Golonzka,
 and Timothy F. Crimmins**

Express Mail No.: EL 990135768 US

Date: March 10, 2004

Prepared by: Timothy Trop, Trop, Pruner & Hu, P.C.
8554 Katy Freeway, Ste. 100, Houston, TX 77024
713/468-8880 [Office], 713/468-8883 [Fax]

EVALUATING THE QUALITY OF A CONTACT PLUG FILL

Background

This invention relates generally to processes for manufacturing semiconductor integrated circuits.

Semiconductor integrated circuits undergo a process 5 called contact plug fill. In this process, a dielectric material is processed. Contact holes or trenches are patterned into the dielectric. These holes or trenches are then filled with a conducting fill material to form contact plugs.

10 In some cases, some of the plugs are well filled with the conducting material, while others may have gaps or seams in them. This is an undesirable feature which may reduce the yield of the resulting semiconductor integrated circuit.

15 Thus, there is a need for ways to evaluate the quality of the contact plug fill.

Brief Description of the Drawings

Figure 1 is an enlarged, cross-sectional view at one stage of evaluation in accordance with one embodiment of 20 the present invention;

Figure 2 is an enlarged, cross-sectional view at a subsequent stage of evaluation in accordance with one embodiment of the present invention;

Figure 3 is an enlarged, cross-sectional view at still a subsequent stage of evaluation in accordance with one embodiment of the present invention; and

5 Figure 4 is an enlarged, cross-sectional view at a subsequent stage of evaluation in accordance with another embodiment of the present invention.

Detailed Description

Referring to Figure 1, a semiconductor wafer may include a substrate 12 covered by a dielectric layer 14. A 10 contact hole or trench 16 may be filled with a plug material 15 which may be any conductive material. In the trench 16 on the left, the plug material has a defect B. The defect arises from incomplete filling of the trench 16.

In order to expose the defect, a basic solution may be 15 applied to the wafer, as indicated by the arrows A. In one embodiment, the basic solution is one that penetrates the poorly filled trenches 16 and etches the substrate 12 underneath those trenches along the <111> crystal direction. In one embodiment, a characteristic V-shaped 20 etched region 20 may be left beneath the contacts in the substrate 12 as shown in Figure 2. An example of one basic solution is potassium hydroxide.

On the other hand, the trench 16 on the right side, with no defects, exhibits no such characteristic etch 25 region 20. The trenches 16 that have the V-shaped etched region 20 do not have adequate electrical contact to the

substrate 12 as a result of the V-shaped etched region 20. The trenches 16 with good fill have excellent electrical contact to the substrate 12.

Referring to Figure 3, a defect may be detected using 5 voltage contrast-based defect inspection in one embodiment. No further processing of the wafer itself may be needed in some embodiments. In order to detect the poorly filled trenches 16, a charge is induced on the surface of the wafer by an electron beam using the probes C and D. The 10 trenches 16 that have good fill have good electrical contact to the substrate 12 and, thereby, dissipate the surface charge, as indicated by the arrow E in Figure 3. The trenches 16 that have poor fill and have the V-groove etched out region 20 under them have poor electrical 15 contact to the substrate 12 and are unable to dissipate the surface charge.

A secondary electron image of the wafer is generated using scanning electron microscopy or electron beam wafer inspection. In a secondary electron image, defective 20 trenches 16 are visually distinct from the good trenches 16 due to the influence of the surface charge on the secondary electron emission. The defective trenches 16 can therefore be detected through this voltage contrast-based inspection technique.

25 Referring to Figure 4, in accordance with another embodiment of the present invention, electrical methods may

be used to detect the defects as well. Subsequent wafer processing forms interconnect metallizations 22. Standard, post processing electrical test techniques may be used to detect the open circuits in the trenches 16 that have poor 5 fill and, consequently, have the V-shaped etched region 20. Thus, a conventional ohmmeter 24 and voltage source 26 may be used in accordance with well established semiconductor wafer electrical testing techniques to locate the defective trenches 16.

10 In some embodiments of the present invention, only a short, inexpensive, process flow may enable testing. The turn-around may quick in comparison to other techniques for testing such wafers. Large amounts of quantitative data may be obtained to evaluate fill characteristics due to the 15 large sample areas that may be examined. Well known contrast microscopy-based defect inspection or electrical techniques may be utilized in some embodiments.

While the present invention has been described with respect to a limited number of embodiments, those skilled 20 in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is: